Unit-1

- 1) Explain Digital signal with diagram.
- 2) Explain Basic and Universal gates with the help of truth table and symbols.
- 3) Explain Exclusive OR and Exclusive NOR gate
- 4) What is Number System and explain their types.
- 5) Explain Binary-to-Decimal and Decimal-to-Binary Conversion.
- 6) Explain 1's complement and o's complement along with example...
- 7) Explain Binary Arithmetic with their operation. Addition Subtraction, Multiplication, Division
- 8) Explain Octal-to-Decimal, Decimal-to-Octal, Octal to Binary and Binary to Octal. Explain application of octal number system.
- 9) What is code and explain their types.
 - i) Straight Binary Code
- ii) Natural BCD code
- iii) Excess-3 code
- iv) Gray code
- v) Hexadecimal code.
- vi) Octal cade
- vii) Alphanumeric Code
- 10) Explain the Error Detecting and error-correcting. Code.
- 11) What is Hamming code and explain it with an example.

Unit-2

- 1) Write a short note on combinational circuit..
- 2) Explain KARNAUGH-MAP representation of logic function
- 3) Explain don't care condition.
- 4) Explain Half-Adder and full-adder
- 5 Explain Half-Subtractor and Full-Subtractor.
- 6) Explain BCD to 7-segment Decoder.

- 7) Write a short note on Encoder.
- 8) Write a short note on Multiplexer.
- 9) Explain Demultiplexer.
- 10) Explain BCD-adder with diagram.
- 11) Explain BCD-subtractor with diagram.
- 12) Explain Arithmetic Logic Unit (ALU)

Unit-3

- 1) Explain sequential circuit.
- 2) Explain 1-Bit memory cell.
- 3) Explain Clock-SR Flip Flop and also explain application of flip flop.
- 4) Explain JKT-Flipflop.
- 5) Explain D-type Flip Flop.
- 6) Explain Shift Register
- 7) Explain application of shift Register. (ii) Parallel to serial
- i) serial to parallel ii) Ring Counter (iv) Sequence Counter
- 8) Write a short note on Asynchronous Counter (Ripple).
- 9) Write a short note on Synchronous Counter (Ripple).

Unit-4

- 1) Explain ideal microprocessor with diagram.
- 2) Differentiate between 8-bit microprocessor and 16-bit microprocessor.
- 3) Explain the data bus.
- 4) Explain address bus and control bus.
- 5) Explain the program counter of microprocessor.
- 6) Write a short note on stack pointer and flag.
- 7) Explain the 8086 microprocessor architecture.

Unit-5

- 1) What is memory interface and Ilo interface?
- 2) Write a short note direct memory access.
- 3) Explain interrupts in 8086 microprocessor.
- 4) what is direct and indirect addressing made?
- 5) Explain relative and index addressing mode.
- 6) What is data transfer instructions?
- 7) Explain bit inherent and bit direct addressing mode.
- 8) Explain arithmetic and logical instruction.
- 9) Explain branch instruction and subroutine instruction.
- 10) Explain bit manipulation instruction.
- 11) Write a short note on assembler and compiler.
- 12) What is programming and debugging tools.?

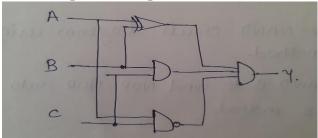
Unit 2

(1 Marks)

- 1. What are the types of Adder?
- 2. What is Arthmetic Logic Unit (ALU)?

(2 Marks)

- 3. How many boolean functions can be defined on n input variables?
- 4. Define sum-of-Product (sop) method.
- 5. Define Product-of- Sum (pos) method.
- 6. Draw NAN-NAND cituit diagram using sop maethod.
- 7. Draw OR- AND Gate and NOR-NOR Gate using Pos method.
- 8. Write a sum--of-products representation of the following circuit.



- 9. What are the universal gates?
- 10. What is Multiplexes & Give an example.
- 11. What are the Multiplexer's uses in Combinational logic DESIGN.
- 12. What are the Standard Ic's. multiplexers. ?
- 13. What is De-Multiplexes? Give an example.
- 14. Draw the block diagram of Demultiplexer.
- 15. Explain the BCD Adder.
- 16. Draw the labelled diagram of One bit BCD Adder.
- 17. BCD Adder.
 - a) 25+17
 - b) 30+65
 - c) 14+12
- 18. Explain the BCD substractor.
- 19. Draw the labelled diagram of one bit BCD Substractor of one bit BED Subtractor
 - 20. BCD substractor.
 - a. 58-32

c. 6-9

- 21. Write the procedural steps for the design of combinational circuits.
- 22. Draw One to two-demultiplexer circuit
- 23. Draw two to one-multiplexes, circuit.
- 24. Draw a parity checker circuit for 3 bit binary word X1 X2 X3.
- 25. Define Parity Generators.
- 26. Make a 9-bit odd parity checker using single 74180 and an inverter.

(3 Marks)

- 1. What are the Standard representation for logic functions & Explain in details. Write each example.
- 2. Given the logic eqn.

$$Y = (A + CB) (A + overline A C)$$

Draw a circuit using gates to realise the funct?

- 3. Find out whether it is possible to design the crecuit with only one type of gates. If yes, draw the circuits (in above example).
- 4. Convert following equations into canonical pos form

a)
$$Y = (A+B)(A+C)(B+C)$$

b)
$$Y = (A + B + C) (A+B+C)(A+B+C)$$

5. Draw k-map representation of logic funct of sop method.

$$y = sum(1,3,6,8)$$
.

6. Draw K-map representation of logic function?.

$$y = pi (2,4,5,9,11).$$

- 7. Representation of Truth Table on k- map using 3-variables. and find sop and pos equation.
- 8. What is combinational Circuit & Give an example
- 9. Draw the block diagram of Digital Multiplexer and Explain it.
- 10. Draw a combinationed logic circuit which can compare whether two bit binary numbers are Same or not.
- 11. Draw the black diagram of Multiplexer with Strobe Input Using NAND gates.

12. Implement the expression using al multiplexes.

$$F(A,B,C,D)=sum\ m(0,1,2,5,6,7,10,13)$$

- 13. Realise the logic function of 16-bits truth table, into 4-variable Truth table using 8:1 multiplexer.
- 14.. Draw the labelled diagram of 74181 ALU and Explain it
- 15. Draw a block diagram of 74180 Parity Generator.
- 16. Make a 16-bit even parity checker using two 74180s

(4 Marks)

- 17. Convert following Equations into canonical SOP form.
 - a) Y=AB + AC + BC
 - b) Y=AB+AC+BC
 - c) Y=ABC+AB+BC
 - d) Y=AB+BC AV
- 18. Implement the following multi-output combinational logic circuit using a 4 to 16-line decoder

$$F1 = Em(0, 1, 2, 3, 7, 9, 13, 14).$$

$$f2 = Em(2, 4, 6, 10, 12)$$

- 19. Realise the functions of four variates using.
 - a) 8:1 multiplexes.
 - b) 16:1 multiplexers.
- 20. Design an 8-bit adder and substractor uing 7418 is in cascade. Show how it works if

a)
$$A = 27$$
 and $B = 94$

b)
$$A = 54$$
 and $B = 15$

(5 Marks)

15. Draw a combinational logic circuit of an eight input multiplexor where the inputs.

Unit 3

(2 Marks)

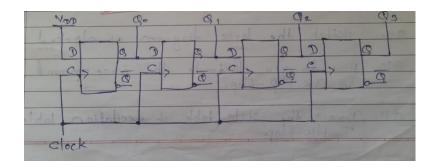
- 01. Mention Difference between the edge triggering & level triggering.
- 02. Write the characteristic equation of a JK flip-flop.
- 03. State difference between Moore & Mealy state machine.
- 04. How many flip-flop are required to builds binary counter that counts from 0 to 1023?
- 05. sketch the logic diagram of clocked SR-FF.
- 06. Draw the state table & excitation table of T-flip-flop.
- 07. Draw the block diagram for Moore model.
- 08. Write a Verilog model of full subtractor circuit.
- 09. Define latch.

(3 Marks)

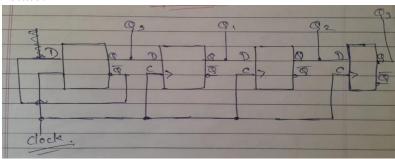
- 1. What is meant by programmable counter?. Mention it's application?
- 2. Realise T-Flip-Flop from JK- flip-flop.
- 3. Convert JK-Flip-flop to T- flip-flop. B-Marks.
- 4. How do you eliminate the ground condition in Jk flip-flop?
- 5. A 4-bit binary ripple counter is operated with clock Frequency of 1kHz. What is the output Frequency of its third flip-flop?
- 6. Realize Jk flip-flop usind D flip-flop.
- 7. Design 3- input AND gate using verilog.

(4 Marks)

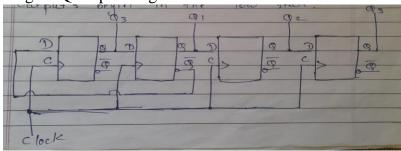
- 1. Compare the logic of synchronous counter & ripple counter.
- 2. Write the VHDL code for half adder.
- 3. Design a 3-bit ring counter and find the mod of designed counter.
- 4. Write short note on Digital clock.
- 5. Complete the timing diagram for this circuit, assuming all Q outputs begin in the low state.



- 6. What is the definition of a register in the context of digital circuitry? Also, define and compare / contrast what is shift register is?
- 7. Complete the timing diagram, For this circuit assuming all Q output begin in the low state:



8. Complete the timing diagram for this circuit, showing propagation delays for all Flip-flops (delay time much less than the width of the clock pulse), assumming all Q outputs begin in the low state.



9. Explain the difference between serial digit dada and parallel digit data.